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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method for configuring an integrated device in a first processor comprising:

converting a configuration access corresponding to a memory address or Input Output (IO) address access within a decoder of a second processor, the second processor coupled to the first processor by a network fabric comprising a plurality of point to point links, to a configuration cycle for configuration of the integrated device in the first processor;

routing the configuration cycle directly from the decoder to the first processor based at least in part on a routing information to configure the integrated device from an unconfigured state to a configured state, wherein an entire configuration space is globally visible to the first and second processors.

Claim 2 (currently amended): The method of claim 1 wherein the configuration cycle is routed via [[a]] the network fabric.

Claim 3 (cancel)

Claim 4 (canceled)

Claim 5 (cancel)

Claim 6 (currently amended): A method for configuring an integrated device in a first processor comprising:

decoding an Input Output (IO) configuration access within a second processor, coupled to the first processor, to a configuration cycle, wherein the decoding includes retrieving a node identifier ~~and a port number~~ using a configuration address associated with the IO configuration access, and retrieving a port number using the node identifier; and

routing the configuration cycle including a transaction address, the node identifier, and the port number directly from the second processor to the integrated device in the first processor based at least in part on a routing information to configure the integrated device from an unconfigured state to a configured state.

Claim 7 (canceled)

Claim 8 (currently amended): The method of claim 6 wherein ~~the~~ a network fabric that routes the configuration cycle is a plurality of point to point links.

Claim 9 (previously presented): The method of claim 6 wherein the configuration adheres to an interconnect of a predetermined protocol.

Claim 10 (previously presented): The method of claim 9 wherein the predetermined protocol comprises a PCI type interconnect protocol.

Claim 11 (currently amended): The method of claim [[6]] 8 wherein the second processor is coupled to the first processor via the network fabric.

Claim 12 (currently amended): A processor comprising:

a decoder to decode either a memory or IO configuration access for configuration of an integrated device of a second processor directly coupled to the processor by a plurality of point to point links to a configuration cycle, wherein the decoder is to receive a configuration address and provide a transaction address, a node identifier corresponding to an address range of the configuration address, and a port identifier corresponding to a range of the node identifier with the configuration cycle; and

to transmit the configuration cycle directly to the integrated device.

Claim 13 (previously presented): The processor of claim 12 wherein the transmission of the configuration cycle to the integrated device is via a PCI type interconnect.

Claim 14 (previously presented): The processor of claim 12 wherein the configuration cycle is to be routed to the integrated device via a network fabric.

Claim 15 (currently amended): A system comprising:

a first processor with a decoder coupled to a second network component with an integrated device, the decoder to decode either a memory or IO configuration access for configuration of the integrated device to a configuration cycle; and

to transmit the configuration cycle directly to the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol and is routed to the integrated device via a network fabric comprising a plurality of point to point links, and wherein an entire configuration space is globally visible to the first processor and the second network component.

Claim 16 (previously presented): The system of claim 15 wherein the first type of interconnect protocol comprises a PCI type protocol.

Claim 17 (cancel)

Claim 18 (currently amended): An article of manufacture comprising:

a machine-readable storage medium having stored thereon a plurality of machine readable instructions, wherein when the instructions are executed by a system, the instructions provide configuration of an integrated device in a processor or network component by:

decoding either a memory or IO configuration access to a configuration cycle in a decoder of a second processor, wherein the decoder is to receive a configuration address and provide a transaction address, a node identifier corresponding to an address range of the configuration address, and a port identifier corresponding to a range of the node identifier with the configuration cycle; and

transmitting the configuration cycle directly from the second processor to the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol.

Claim 19 (currently amended): The article of manufacture of claim 18 wherein the integrated device is coupled to the decoder of the second processor coupled to the processor or network component via a network fabric having a plurality of point to point links.

Claim 20 (previously presented): The article of manufacture of claim 18 wherein the first type of interconnect protocol is in accordance with a PCI type protocol.

Claim 21 (canceled)